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				Application Number	09/849658
				Filing Date	5/4/2001
				First Named Inventor	G. Glenn Henry
				Group Art Unit	2181
				Examiner Name	Tonia Meonske
				Attorney Docket Number	CNTR.2022
Sheet	1	of	1		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ^{2(a)(known)}			
TM		8888444	11-22-2006	Kroesche et al.	
TM		8725357	04-20-2004	Jean Philippe Cousin	
TM		8041406	03-21-2000	Thomas S. Green	
TM		8754808	06-22-2004	Roth et al.	
TM		8374350	04-18-2002	D'Sa et al.	
TM		8434985	07-18-1996	Emma et al.	
TM		5553248	08-03-1996	Hiromi Suzuki	
TM		8122729	08-19-2000	Thang M. Tran	
TM		8748441	08-08-2004	David James Gemmell	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TM	AA	The D Latch, Play-Hockey Web Page, Oct 10, 1999.	
TM	AB	Patterson et al. "Computer Organization & Design: The Hardware/Software Interface." Morgan Kaufmann Publishers, Inc. San Francisco, CA. 1988 Page 489 SECOND EDITION	
TM	AC	Jimenez et al. "The Impact of Delay on the Design of Branch Predictors." 2000 Pgs 1-10 IEEE	

Examiner Signature	<i>Tonia Meonske</i>	Date Considered	June 12, 2006
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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

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		Number-Kind Code ² (known)			
TM		6321321	11-20-2001	Mark W. Johnson	

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. IBM TECHNICAL DISCLOSURE BULLETIN		
TM	AA	EBERLY et al. "The Correlation Branch Target Address Cache" May 1998, pgs 83-85, VOL. 39 NO. 5.		
TM	AB	Patterson et al. "Computer Organization & Design: The Hardware/Software Interface." Morgan Kaufmann Publishers, Inc. San Francisco, CA. 1998 Page 463-466 SECOND EDITION		

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